REMARKS/ARGUMENTS

Status of Claims

In the Office Action, Claims 1-20 were noted as pending in the application and all claims were rejected. In addition, the drawings filed on June 24, 2003 were found objectionable.

By the present amendment, it is submitted that drawings have been amended as necessary to overcome the objection to the drawings. In addition, it submitted that the claims have been amended as necessary to overcome the objection and rejections to the same under 35 U.S.C. §112, Second Paragraph. Further, it is submitted that Claims 1-20 are patentable over the prior art.

The rejections and objections are specifically addressed below.

Objections to the Drawings

On Page 2, Item 1 of the Office Action, the drawings were objected to under 37 C.F.R §1.83(a). Specifically, the drawings were found objectionable because the passivation layer, rectifying contacts, heterojunction, sidewalls, dummy gate, and gate-insulating-film-forming layer, were not shown or numbered in the drawings.

By the present Amendment, approval of drawing changes is requested to specifically label the passivation layer shown in the drawing, as element "7". In addition, approval is requested of the labeling of the "side walls 8" of the gate insulating layer 3. Support for these drawing changes is found in the Drawings, Paragraphs [0010]-[0011] of the Specification, and Claims 10, 11, 16, and 20 as originally filed.

In addition, throughout the specification, the terms "electrode" and "contact" are used interchangeably. By the present Amendment, all occurrences of "electrode" have been changed

to "contact" for consistency throughout the specification and drawings. Similarly, throughout the specification, "film" and "layer" are used interchangeably. By the present Amendment, all occurrences of "film" have been changed to "layer" to consistently refer to the corresponding element throughout the specification and drawings.

Claims 16 and 20 have been canceled without prejudice, rendering it unnecessary to indicate the other elements specifically recited therein in the drawings to the extent the features are not recited in other Claims. Approval of the attached drawings changes is requested.

On Page 2, Item 2 of the Office Action, the drawings were found objectionable for not complying with 37 C.F.R. § 1.84(p)(4) because the reference character "6" has been used to designate both the gate insulating film and the channel layer. Applicant interprets the Examiner's comments as meaning that the channel layer "3" should be changed to the "channel layer 2" in Paragraph [0017] of the specification. The drawings correctly refer to the "channel layer" as element "2" so no further amendment of the drawing is required to comply with this objection.

Claims Objections

On Page 3, Item 3 of the Office Action, Claim 4 was found objectionable due to unnecessary period punctuation in the recited range of values for the variable "x". By the present Amendment, it is submitted that Claim 4 has been amended as necessary to overcome the objection.

Rejection of Claims 9-11, 14, 16, and 20 under 35 U.S.C. §112, Second Paragraph

On Page 3, Items 4 and 5 of the Office Action, Claims 9-11, 14, 16, and 20 were rejected under 35 U.S.C. §112, Second Paragraph. By the present Amendment, it is submitted that Claims 9-11 and 14 have been amended as necessary to overcome the rejection of these Claims.

Claims 16 and 20 have been canceled without prejudice so that the rejection of these Claims is moot. Withdrawal of the rejection is requested.

Rejection of Claims 1- 9, 11-13, 16, and 17 under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457)

On Page 4, Items 6 and 7 of the Office Action, Claims 1-9, 11-13, 16, and 17 were rejected under 35 U.S.C. § 103(a) based on the Suzuki and Wolter patents. The Suzuki and Wolter patents, and the reasons that Claims 4-9, 11-13, 16, and 17 are patentable over the prior art, are addressed below.

Suzuki discloses semiconductor device which comprises a channel layer 13 (n-type GaAs), a gate electrode 21 (Al or Au), and a barrier layer 17 (AlAs). Suzuki also discloses that the barrier layer 17 can be composed of $Al_cGa_{1-c}N$, in which case the channel layer 13 must be composed of $In_{1-d}Ga_dN$ (Suzuki, column 7, line 57 – column 8, line 47). Thus, Suzuki as properly interpreted discloses a barrier layer 17 composed of a Group III nitride compound semiconductor disposed on a channel layer 13 which is also a Group III nitride compound semiconductor. Thus, Suzuki fails to disclose "a channel layer" being composed of II-VI compound semiconductor zinc oxide, and "a gate insulating layer" disposed between a gate contact and the channel layer which is composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure," as recited in Claim 1 as amended. In the case of the channel layer being formed as a Group-III nitride, this feature of the claimed invention induces strain between these layers of the transistor, resulting in formation of a two-dimensional electron gas. Not only does Suzuki fail to teach the claimed invention, it "teaches away" from it by disclosing that Group III nitrides should be used together. Moreover, in the case of the channel layer being composed of MgZnO quantum well structure, Suzuki contains no mention of a channel layer composed of ZnO or a gate insulating layer composed of MgZnO, as recited in Claim 1 as amended. Thus, for these reasons as well as for

those stated above with respect to Claim 1 as amended, it is submitted that Claim 1 as amended is patentable over the prior art.

Wolter fails to overcome the deficiencies of Suzuki. Wolter is relied upon as disclosing use of ZnO as a possibility for a material to be used to create a two-dimensional electron gas in a HEMT device. However, in column 7, line 57-column 8, line 8, Wolter expressly states:

> Suitable materials are, for instance, other III-V components and mixed crystals thereof, for example InP, InAs, InSb, GaP, GaSb, etc., II-VI compounds and mixed crystals thereof, for example CdSe, CdTe, CdS, ZnSe, ZnO, etc., **or** elementary semiconductors such as Ge and Si. *Emphasis added.*

Thus, properly interpreted, Wolter teaches that Group III-V compounds or mixed crystals, or Group II-VI compounds or mixed crystals thereof, or elementary semiconductors, can be used to form its semiconductor device. Wolter does not state that materials from Group II-VI like ZnO or MgZnO should be used with Group III-V materials like Group III-nitrides. Suzuki and Wolter, whether considered alone or in combination, fail to disclose a channel layer composed of a II-VI compound semiconductor zinc oxide combined with a gate insulating layer composed of Group III-nitride compound semiconductor or a magnesium zinc oxide (MgZnO) quantum well structure, or both. Thus, because both Suzuki and Wolter "teach away" from the claimed invention, their combination is respectfully traversed because a person of ordinary skill would not have been motivated to combine them. In addition, it is submitted that Claim 1 as amended would not have been obvious to a person of ordinary skill in the art considering these patents whether alone or in combination because such patents "teach away" from the claimed invention and thus fail to disclose it. Therefore, it is submitted that Claim 1 as amended is patentable over the prior art.

Claims 2-9 and 11-13 depend, directly or indirectly, from Claim 1 as amended and include all limitations of that Claim plus additional limitations that are not disclosed in the prior art. For example, Claim 4 recites certain ranges for the chemical composition of the gate

insulating layer formed on the channel layer of zinc oxide (ZnO), that are not disclosed in the prior art. In addition, Claim 5 recites chemical compositions for the substrate supporting the channel layer, that are not disclosed in the prior art. Claim 6 recites that the gate insulating layer ranges from 0.30 to 50 nanometers. The prior art does not disclose a gate insulating layer of Group-III nitride or MgZnO disposed on a ZnO channel layer, let alone one having the recited range of thickness. Claim 7 is directed to use of piezoelectric doping created by strain due to crystal lattice mismatch between the Group-III nitride and/or MgZnO gate insulating layer and the ZnO channel layer, a feature that is not disclosed in the prior art. Claim 8 recites that the gate contact has certain chemical compositions. The prior art fails to disclose a gate contact formed on a Group-III nitride and/or MgZnO gate insulating layer formed on a ZnO channel layer, let alone a gate contact with the recited composition. Claim 9 recites source and drain contacts composed of certain chemical compositions in contact with the ZnO channel layer. The prior art fails to disclose the recited structure with Group-III nitride and/or MgZnO gate insulating layer, let alone the further limitation of source and drain contacts with the recited compositions. Claim 11 recites that the gate contact is bounded by side walls of the gate insulating layer. Although Wolter discloses a mesa-shaped part with sidewalls, such sidewalls pertain to a semiconductor layer, not a gate insulating layer. Thus, this feature recited in Claim 11 is not disclosed in the prior art. Claim 12 recites the area of the gate contact with the gate insulating layer is decreased due to the presence of sidewalls of the gate insulating layer. Suzuki and Wolter fail to disclose any side walls for the gate contact of their semiconductor devices, which provide additional gate insulation and can be used as a mask to form holes for source and drain contacts to the channel layer to simplify manufacturer of the claimed transistor. Claim 13 recites that the channel layer composed of ZnO is grown by metal organic chemical vapor deposition (MOCVD). While in general MOCVD is not a new technique, its use to grow a ZnO channel layer in combination with forming a gate insulating layer of Group-III nitride and/or MgZnO is submitted to be nonobvious to a person of ordinary skill in the art. Thus, for this reason as well as for those stated above with respect to Claim 1 as amended, it is submitted that Claims 2-9 and 11-13 are patentable over the prior art.

Claim 17 recites steps of defining a channel layer composed of a II-VI compound semiconductor zinc oxide; forming a gate contact disposed on the channel layer; and forming a gate insulting layer disposed between the gate contact and the channel layer and composed of Group-III-nitride and/or a MgZnO quantum well structure. Suzuki and Wolter fail to disclose this method, but instead "teach away" from it by effectively stating that two layers of a semiconductor device can be composed of same-Group selections of certain Group II-VI compounds, Group III-V compounds, or Group IV elements, implying that different Groups should not be used together to form its semiconductor layers (e.g., see Suzuki, column 7, line 57 – column 8, line 47; Wolter, col. 7, line 65 – column 8, line 2). Wolter contains no mention of a gate insulating layer, let alone one composed of a Group III-nitride and/or MgZnO, so it would not have been obvious to a person of ordinary skill in the art how it could be combined with Suzuki in an effort to obtain the claimed invention. Neither Suzuki and Wolter contain any mention of MgZnO, let alone its use in forming a gate insulating layer, especially not in connection with defining a ZnO channel layer. Accordingly, the combination of Suzuki and Wolter is respectfully traversed, and it is submitted that Claim 17 is patentable over the prior art for at least the above-stated reasons.

Claim 16 has been canceled without prejudice so that the rejection of this Claim is moot.

Rejection of Claim 10 under 35 U.S.C. § 103(a) based on Suzuki and Wolter, in further view of Shanfield (U.S. Patent No. 5,880,483)

On Page 5, Item 8 of the Office Action, Claim 10 was rejected under 35 U.S.C. §103(a) based on the combination of Suzuki, Wolter and Shanfield. Claim 10 depends from Claim 1 as amended and includes all the limitations of that Claim. Shanfield fails to disclose the deficiencies of Suzuki and Wolter as noted above with respect to the rejection of Claim 1 as amended under 35 U.S.C. §103(a). More particularly, Shanfield discloses formation of a passivation layer over gate, source and drain contacts, but not of a transistor having a channel layer composed of II-VI compound semiconductor zinc oxide and a gate insulating layer

composed of Group III nitride compound semiconductor or a magnesium zinc oxide quantum well structure, as recited in Claim 10 as amended. Accordingly, it is submitted that Shanfield too "teaches away" from Claim 10 and its combination with Suzuki and Wolter is thus respectfully traversed because a person of ordinary skill would not have been motivation to combine teachings of these patents. Thus, it is submitted that Claim 10 would not have been obvious to a person of ordinary skill in the art, and therefore patentably distinguishes over the prior art.

Rejections of Claims 14, 15, and 19 under 35 U.S.C. § 103(a) based on Suzuki, Wolter and Nishikawa (U.S. Patent No. 6,323,053)

On Page 6, Item 9 of the Office Action, Claims 14, 15 and 19 were rejected as being unpatentable over the combination of Suzuki, Wolter and Nishikawa. Although Nishikawa discloses a method of forming a semiconductor layer of gallium nitride (GaN) on a substrate 11 that can be a c-surface zinc oxide (ZnO) substrate (see, e.g., Nishikawa, column 11, lines 50-55), Nishikawa does not disclose the c-surface ZnO substrate in the context of a transistor with a channel layer composed of II-VI compound semiconductor ZnO, and a gate insulating layer composed of a Group–III nitride compound semiconductor or magnesium zinc oxide (MgZnO) quantum well structure, or both, as recited in independent Claim 1 as amended from which Claims 14 and 15 depend. Similarly, Claim 19 depends from independent Claim 17 which recites steps of defining a channel layer composed of a II-VI compound semiconductor zinc oxide, forming a gate contact based on the channel layer, and forming a gate insulating layer between the gate contact and the channel layer, which is composed of a Group–III nitride compound semiconductor, magnesium zinc oxide (MgZnO) quantum well structure, or both, and further, that the ZnO channel layer is formed on a c-surface ZnO substrate. Instead, in Nishikawa, a GaN semiconductor layer is formed directly on the ZnO substrate, thus "teaching away" from Claims 14, 15, and 19 which recite a ZnO channel layer formed on a c-surface ZnO substrate. Thus, the combination of Suzuki, Wolter and Nishikawa is respectfully traversed not only for the reasons previously stated with respect to Suzuki and Wolter, but also because Wolter "teach away" from the claimed invention by disclosing that a GaN semiconductor layer should

be formed on a c-surface ZnO substrate. Thus, neither Suzuki, Wolter, Nishikawa, nor any combination of the same, contain any suggestion of forming a ZnO channel layer on a c-surface ZnO substrate in the context of the recited transistor of Claims 14 and 15 or the method of Claim 19. Thus, it is submitted that Claims 14, 15, and 19 patentably distinguish over the prior art.

Rejection of Claim 18 under 35 U.S.C. § 103(a) based on Suzuki, Wolter, and Ando (U.S. Patent No. 6,429,467 B1)

On Page 6, Item 10 of the Office Action, Claim 18 was rejected under 35 U.S.C. §103(a) based on Suzuki, Wolter, and Ando. Ando is relied upon as disclosing a gate insulating layer formed using a metal organic chemical vapor deposition (MOCVD) technique. However, Ando fails to disclose the formation of a gate insulating layer composed of a Group-III nitride compound semiconductor or magnesium zinc oxide (MgZnO) quantum well structure, or both, in connection with a channel layer composed of a Group II-VI compound semiconductor zinc oxide. Thus, Ando "teaches away" from the claimed invention, and there is thus no motivation that would have led a person of ordinary skill in the art to combine Suzuki, Wolter, and Ando in an effort to obtain the claimed invention. Accordingly, the combination of the Suzuki, Wolter, and Ando patents is respectfully traversed. In addition, it is submitted that Claim 18 patentably distinguishes over the prior art which does not disclose forming a gate insulating layer of the recited kind using MOCVD in the context defined by the limitations of Claim 18. Thus, it is submitted that Claim 18 as amended patentably distinguishes over the prior art.

Rejection of Claim 20 under 35 U.S.C. § 103(a)

On Page 7, Item 11 of the Office Action, Claim 20 was rejected under 35 U.S.C. §103(a). By the present Amendment, Claim 20 has been canceled without prejudice so that the rejection of this Claim is moot.

Miscellaneous

All amendments not specifically relied upon for patentability are made for purposes of improving the form of the Claims and specification only. For example, changing the term "electrode" to "contact" and "film" to "layer" throughout the specification and Claims is made for the purpose of consistent reference to these elements, and is not made for purposes of securing patentability of any Claims affected by these amendments. Thus, reservation of the right to Claim the full scope of equivalents permitted by law is retained with respect to such amendments.

Conclusion

It is submitted that the drawings have been amended as necessary to overcome the objection to the same. Also, it is submitted that Claim 4 has been amended as necessary to overcome the objection. Further, it is submitted that Claims 9-11 and 14 have been amended as necessary to overcome the rejection under 35 U.S.C. §112, Second Paragraph. Moreover, it is submitted that Claims 1-15 and 16-19 have been amended as necessary to overcome the rejections under 35 U.S.C. §103(a). The combination of patents relied upon in the rejections is respectively traversed due at least to the fact their disclosures "teach away" from each other and the claimed invention. Certain amendments have been made to the specification and Claims for the purpose of improving their form, and were not made for reasons of patentability, preserving the right to claim equivalents for elements so amended in the Claims. Claims 16 and 20 have been canceled without prejudice so that the rejection of these Claims is moot. Accordingly, reconsideration of Claims 1-15 and 17-19 as amended and an early Notice of Allowance for all pending Claims, are earnestly solicited.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required

therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

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Amendments to the Drawings:

In the attached Replacement Sheets, the Drawings have been amended to indicate the "passivation layer 7" and the "side walls 8" of the gate insulating layer 3. In addition, the various elements have been labeled with the terms used to reference them in the Specification and Claims. Approval of these drawing changes is requested.